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DESIGN AND FABRICATION OF HIGH SPEED CARDS FOR THE TRANSIENT ANNEALING TEST SYSTEM (TATS)

May 1990

CONTRACT: N00014-88-C-2081
$72,741.00
(NON-COMPETITIVE)

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BACKGROUND

The manner in which the I/V curves change during and after irradiation is a complex function of many factors, most of which have some type of very fast and/or logarithmic behavior with time. For example, in CMOS/SOS technologies as well as bulk CMOS technologies with planar hardened field oxides (no guardbands), a leakage path under the field oxide, around the end of the gate, may result in IC failure after a short pulse, high dose exposure. As the charge trapped in the field oxide anneals with time, the leakage current will decrease and finally disappear.

The Transient Annealing Test System (TATS) was developed to study the time varying I/V characteristics of MOSFET and BIPOLAR transistors following exposure to radiation so that phenomena such as that described above could be investigated. The TATS (see figure 1) is a modular system that accepts up to eight plug-in card sets, each set being essentially an independent test system. There are a number of types of measurement channels that can be selected and combined in one box to allow for the simultaneous measurement of a number of parameters. For instance, one channel might be used to measure I/V curves on an FET and another channel might be used to record the time varying capacitance/voltage curves of a test capacitor. The control unit, which contains the plug-in cards, was designed to be located in the radiation facility and controlled remotely for a PC over an RS-232 link.

The original TATS system was able to measure I/V curves at a rate of one point every 75uS and to switch between annealing and test biases in approximately 200uS. This speed was sufficient to measure many types of failure mechanisms, but it was determined that much more information could be gained if the I/V sweeps could be performed faster.

The work under this contract was to design and build a plug-in module for the TATS box which would perform the same functions as the original TATS, but which would be much faster. In addition, it was desirable that the new, faster channels would be compatible with other TATS cards so that any combination of measurement channels could be utilized for any test.

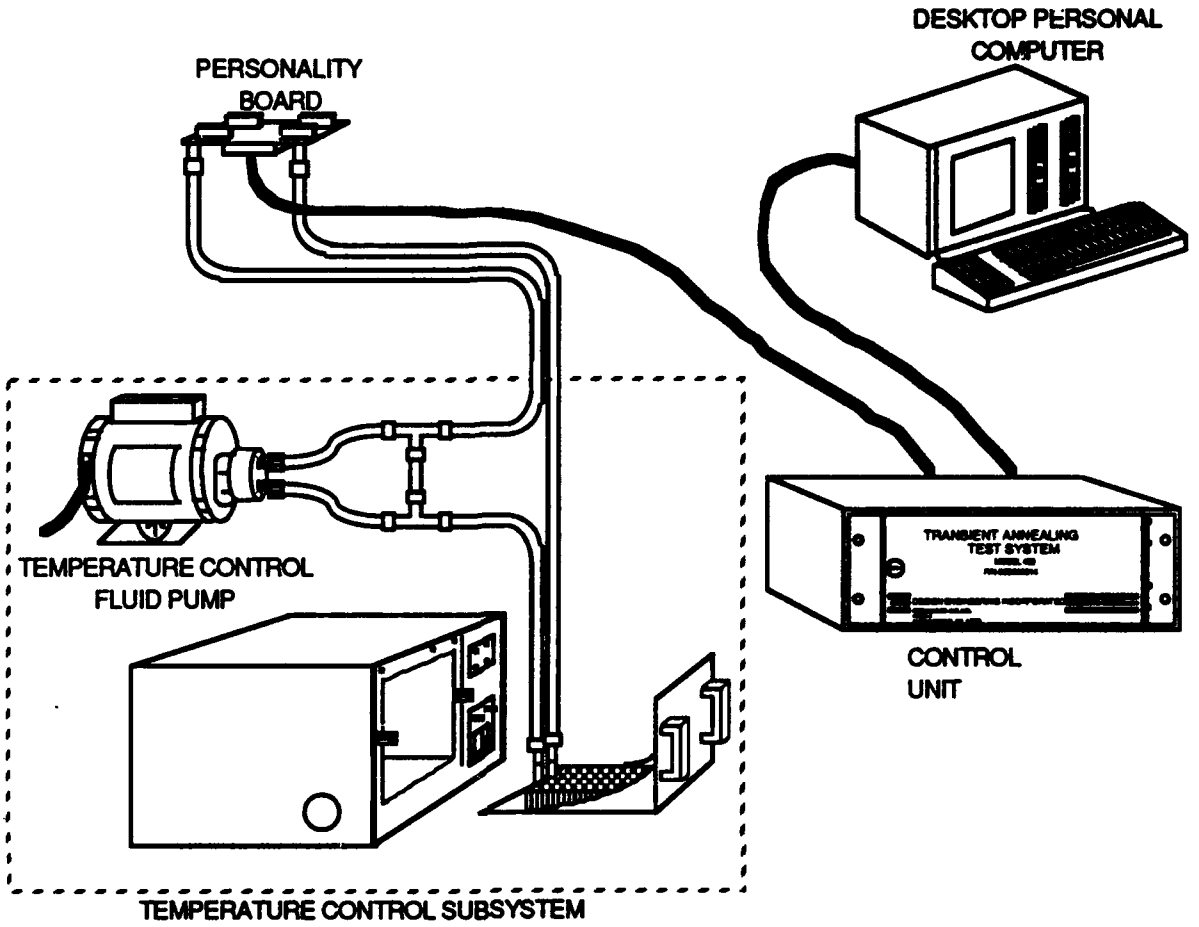

FIGURE 1 - OVERVIEW OF TATS SYSTEM

A lot of effort was expended under this contract developing techniques to optimize measurement speed. One particular difficulty was in developing an understanding of the way the electrical characteristics of FETs varied over the full range of bias conditions and how this affected the dynamic characteristics of the biasing circuitry. Knowledge developed from this effort resulted in circuitry which is considerably different from original concepts for a fast TATS card.

Specifications for the fast measurement channels which were developed are as follows:

Measurement Speed: A sweep can start as early as 10uS after system trigger and other sweeps can be delayed up to 24 hours with a 32uS resolution.

During a sweep the system can measure one I/V point every 1.75uS.

There is a programmable delay (settling time) between when a current is forced and the gate voltage read. Each decade of current can be programmed separately n a 1-2-5 sequence from 1.75uS to 64uS.

Test Conditions: The system can force approximately 2000 logarithmically spaced currents between 1nA and 1mA (either polarity). There are a programmable number of source currents per sweep and a programmable number of drain voltages per sweep start time.

Part Biasing: Gate, drain, source and substrate biases are separately programmable with 12-bit accuracy. The programmable gate range is +/-20V and the other biases have a range of +/-10V.

Gate Voltage Measurement Specifics: Servo the gate over the range of +/- 20 volts to maintain the desired source voltage and measure the resultant voltage with a precision of 10mV.

Compliance Limit: Programmable maximum gate voltage limit with a precision of ~0.2V.

This report details the design of the new fast TATS measurement cards. For discussions concerning programming and operation of the cards, it is assumed that the reader is already familiar with the main TATS system.

OVERVIEW OF DESIGN

Conceptually, the fast TATS cards are similar to the original design. There is a two card set, an IVDB card contains the analog circuitry for two channels of measurements and separate MEASUREMENT cards contain the digital circuitry and microprocessor controllers. Each MEASUREMENT card communicates separately with the remote control computer, performs detailed control of the channels circuitry, formats measured data, etc. Data points are measured by forcing a source current and measuring the resultant gate voltage.

The design was changed considerably over the original design in the way several functions are implemented. In general the changes were to reduce the amount of involvement the on-card microprocessor has with measurements, and to speed up the way the analog circuitry works. Specifically, the design was changed to include the following features:

Separate Test/Anneal DACs - When programming the TATS system for a test, the operator can have one set of bias conditions applied to the DUT pins before irradiation, another after irradiation, and a third during I/V testing (And the anneal/test bias conditions can be changed for every sweep group). In the original design, there was one DAC for every DUT pin and the on-board processor would program the various biases at appropriate times. Since this was a sequential operation, it took considerable time to convert from one set of bias conditions to another. Also, by changing one bias before another, a transient condition would sometimes be induced that would interfere with measurements. In the new design, each pin has two DACs ... one for pre-radiation and annealing bias and a second for test bias. When a test starts, an analog switch is used to instantaneously change all the pin biases simultaneously.

True Constant Current Source - The original design incorporated sense resistors in the source lead and a servo amp that would control the voltage on the end of the resistor string to set the source current.

A separate servo loop would set the gate voltage to maintain the source voltage at some desired point. The two servo loops were connected with a "feed forward" capacitor to maintain stability. In our work under this contract, we discovered that the two servo loop design was inherently slow. We devised a true constant current source (the same current for a wide range of source voltages) to set the source current. The new design has only one servo loop ... to vary gate voltage and maintain a constant source voltage.

Tight Vg Servo Loop - Integrated circuit op amps have significant propagation delay (group delay). To optimize the settling time of the Vg loop, we chose a design which utilizes a single op amp. In order to achieve the +/- 20 volt range and still maintain the desired speed, we added a voltage gain stage comprised of discrete components.

Cache Memory With State Machine Controller - The speed of the original design was primarily determined by the speed at which the microprocessor could read the desired bias conditions out of memory, program the appropriate DACs, read and store the results. In this design, a separate cache memory is provided which is directly tied to the hardware. When the MEASUREMENT card receives a test file from the controlling computer, the microprocessor un-packs the test data and loads the cache memory with appropriate bias information. At an appropriate time, the processor initiates a sweep by performing a single write to a hardware address. The information in the cache RAM is used to sweep the bias on the DUT and to store the resultant measured data. After a sweep is over, the processor reads the measured data from the cache RAM and transmits it back to the system controller. The detailed timing of each sweep is performed by a programmable state machine chip.

DESIGN DETAILS

A simplified circuit for the measurement card is shown in figure 2. The microprocessor writes anneal and test biases to two separate DACs. The appropriate DAC output voltages are selected and routed to the DUT via an analog switch depending on whether the system is in a test or anneal condition.

The microprocessor loads the desired Is(Force) conditions into a cache RAM. Whenever a test is run, this information is output to a fast DAC. Every time a new bias is loaded into the DAC, a fast ADC is triggered and reads the current gate voltage. This voltage is written back into the cache RAM at the same address as the latest bias condition. An address counter automatically increments the 13 bit cache address every time the microprocessor writes into the cache RAM (when loading bias conditions or reading data) or every time a sweep I/V point is measured (during a test). A state machine controller handles the detailed timing of the hardware signals during a sweep.

It should be noted that the microprocessor data bus is 8 bits wide but the cache data bus is 16 bits wide. Since the data for the DAC and from the ADC are both 12 bits wide, there were four additional bits that could be used for other purposes. We use three of the bits to program a delay (settling time) for every I/V point, and the fourth bit to signal the state machine when a single sweep ends. Bi-directional I/O buffers handle the interface between the two busses.

Because the ADC is triggered simultaneous with a bias condition being loaded, every sweep requires one extra read/write cycle than the number of bias points. Specifically, the very first read/write cycle will load the first desired bias into the fast DAC and will write unknown data back into it's respective memory location. The last cycle will write 0 volts into the DAC and write the the data from the next to last write cycle (the real desired last bias point) into the address location. The process of adding an extra read/write cycle, interpreting data correctly, etc is handled automatically by the system and is mentioned here to explain the waveforms seen if an oscilloscope is used to observe a part while it is being tested.

The schematic for the fast measurement board is shown in drawing 02X000113.

The microprocessor portion of the design consists of integrated circuits U25 through U29. The processor communicates via RS-232 through U12 (level translator). External trigger events are input through U13.D. The processor detects (on power up) which slot it occupies in the control unit by reading the three pins CRDADR 0-2.

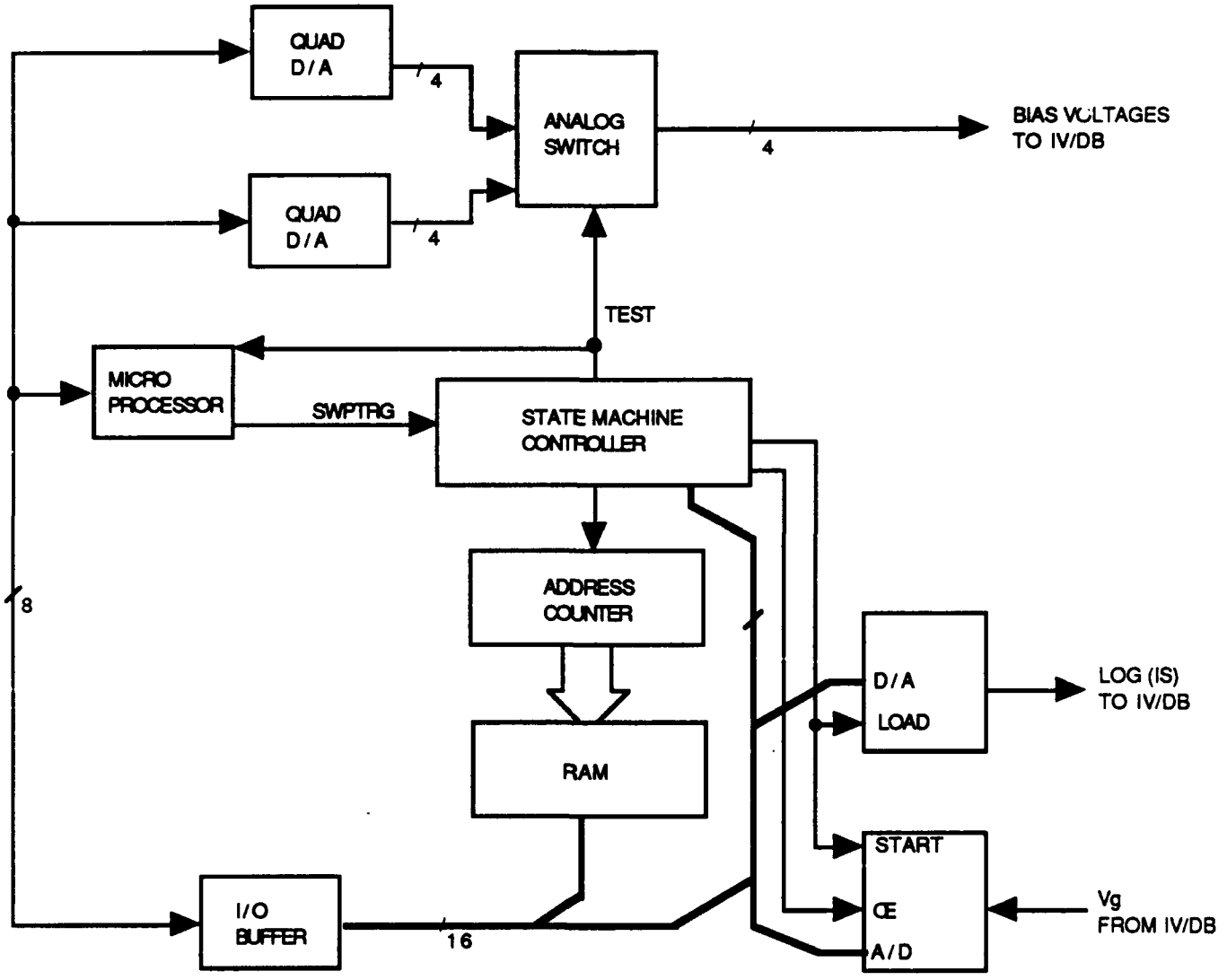

FIGURE 2. FAST MEASUREMENT CARD - BLOCK DIAGRAM

Hardware circuitry on the card is memory mapped into the upper 1/8 of the 16 bit address space of the processor (E000 to FFFF). When write or read operations occur in this range, U17 disables the processor RAMs and enables data selectors U15 and U16. These in turn select the appropriate hardware device.

U21 and U22 comprise the two quad DACs which provide annealing and test biases for the parts under test. U21 provides the pre-radiation and the annealing biases. U22 provides the test voltages for the source drain and substrate pins and the Vg-limit voltage. The outputs of the two DACs go through U18 and U19, two analog switches which are alternately selected depending on the test or annealing state of the board.

The cache memory for rapidly performing I/V sweeps is contained in U5 and U6. The processor writes the Is-force data into these memories and later reads the measured Vg from them. U9 and U10 comprise the 13 bit address counter that is used to sequentially load to or read from the cache RAMs. U11 is the state machine controller which provides the detailed timing of all cache operations (see below).

Bias data from the cache RAMs is latched into U3 and U4 which in turn cause the D/A convertor, U1 to output a voltage. Simultaneous to data being loaded into the D/A latches, the A/D convertor U2 is triggered and reads the analog gate voltage. Data from the A/D convertor is written back into the cache RAMs shortly thereafter and the address incremented.

The equivalent circuit of the state controller is shown in figure 3. The processor loads 8 bit data into the cache RAMs by writing to one of the hardware addresses LDL* or LDH*. This will cause one of the two signals GABL or GABH to go high, selecting one of the two bi-directional data selectors U7 or U8 to transfer processor data to the cache RAMs. These write operations will also cause OEN* to go high, placing the cache RAMs in a high impedance state and will generate either WRL* or WRH* which will write the data into the cache RAMs. The trailing edge of the lower byte write (WRL*) will cause the signal CLKOUT to increment the address counters of the cache. Either of these write operations will also have the effect of re-setting an R-S flip-flop which determines if the cache circuitry is in the idle mode or doing a sweep. Essentially, a processor write to cache memory will cause SWPEND to go true. This will in turn force the state machine portion of the design to go into a wait mode .

Note that both forced currents and measured data have 12 bit resolution. The other four bits come into the state machine and program it in two respects, inputs I0, I1, and I2 determine the delay

for a given forced current, and input I3 determines the end of each sweep.

When the processor determines that it is time for a sweep, it programs SWPTRG* low momentarily. This will cause the R-S flip-flop to change states and will also latch whatever polarity of signal is presently on I3 into a D latch. Since the output of the latch is exclusive-Nor'd with the signal on I3, the internal node X)! will be high. On successive memory force/measure cycles of the sweep, the bit information at I3 will remain constant (either one or zero). At the end of the sweep, I3 will change states causing X01 to go low, SWPEND to go high, and the sweep to terminate.

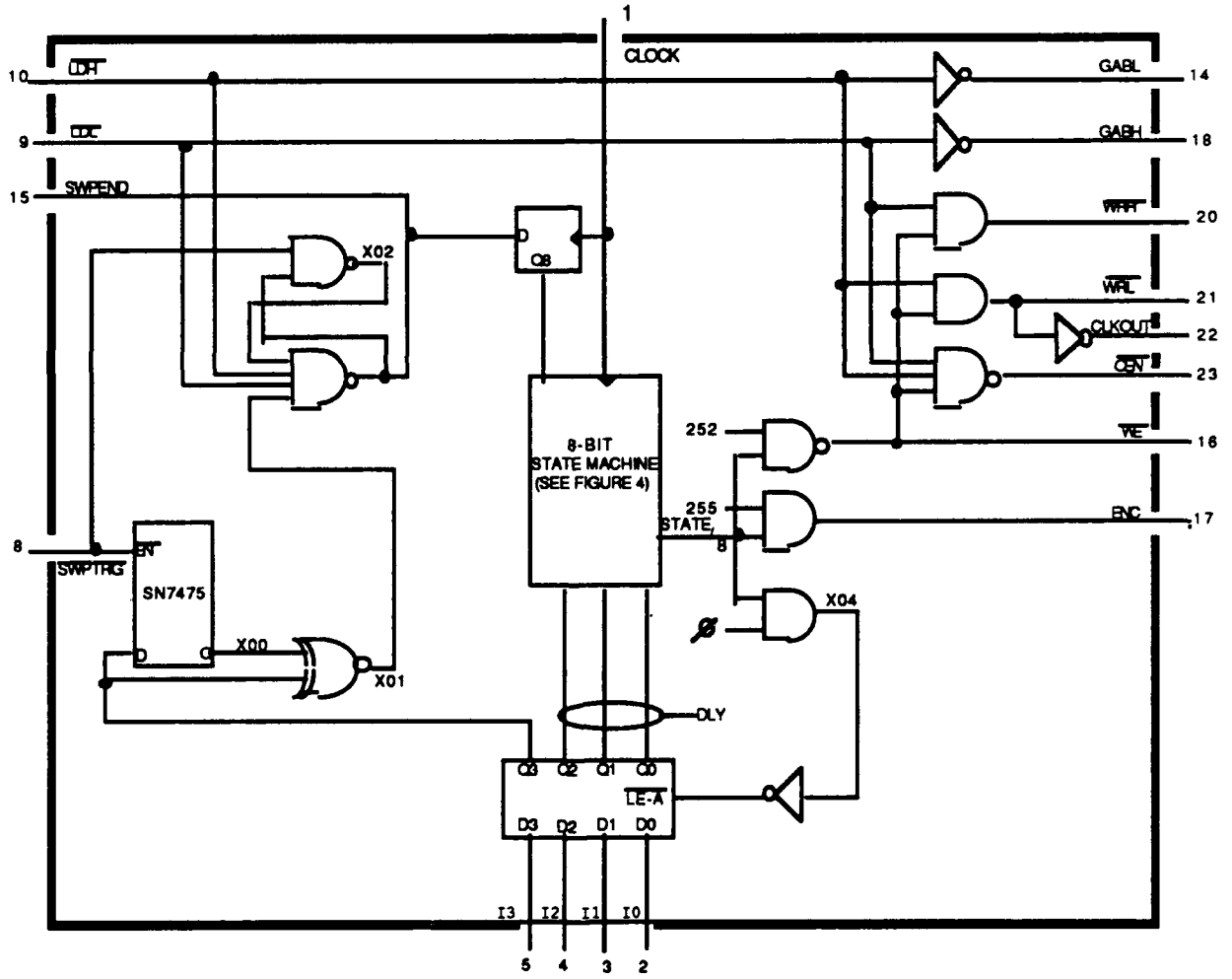

FIGURE 3. STATE MACHINE CONTROLLER - OVERVIEW

The state portion of the design is shown as a flow diagram in figure 4. Note that as long as the state is zero and Q8 (SWPEND) is

high, the system will continuously loop on itself with the internal signal LE_A being low. As soon as Q8 goes low, the system will transition to state 255 with LE_A going high (freezing the four memory inputs for the rest of the force measure cycle) and also with ENC going high (strobe data into the D/A and initiate an A/D conversion). The system will then progress through several states on successive clock cycles until it reaches 251 at which time the A/D convertor output will be enabled and it's data written into the cache RAMs. From state 251 the system will take one of several vectors depending on the information contained in the (latched) data from I0 -- I3. Basically, the branch taken will determine the number of clock cycles the machine must take to get back to state 0 and will thus determine the settling time before the next possible D/A and A/D strobe.

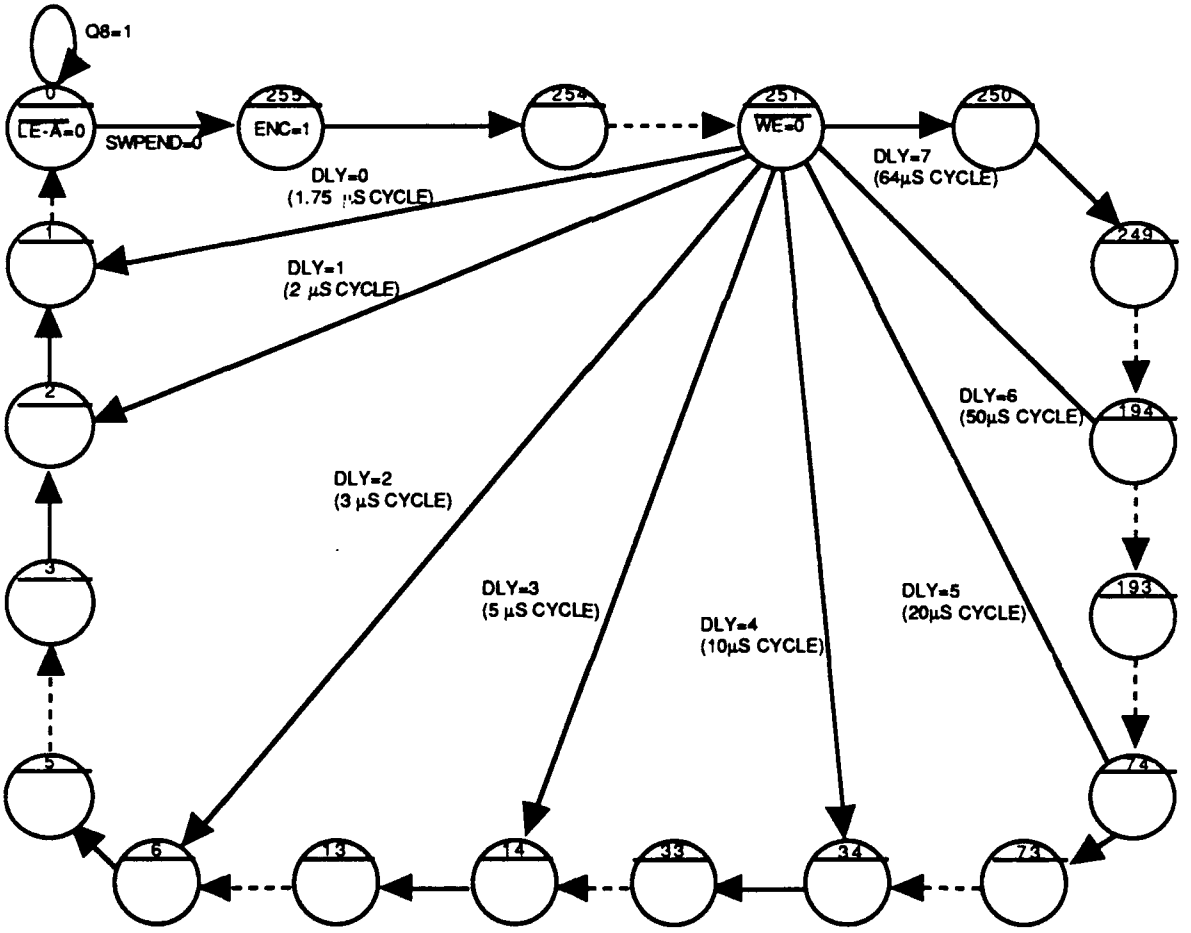

FIGURE 4. STATE MACHINE STATE DIAGRAM

A schematic diagram of the FAST IVDB board is shown in drawing 02X000118.

The IVDB board consists of a +/- 25 volt power supply and two identical force current/servo voltage circuits.

The 25 volt supply is basically a dual voltage doubler which converts 15 volts to the higher voltages. Three gates of U7 provide a clock for the doubler and a fourth provides a delayed clock to the doubler circuit to limit in-rush current load on the +/-15 volt supplies. Once the clock is enabled to pass through U7.B, transistors Q9 and Q10 are alternately turned on which causes an AC voltage to be applied across C29 and C30. The pumping action of this AC voltage , coupled with the blocking action of diodes D8 -- D11 generates the doubled voltages. Several volts are lost in the doubling process due to diode turn on characteristics, transistor saturation resistance, etc.

The overall operation of the force current/servo voltage circuits can best be understood by first looking at figure 5. This simplified block diagram of the circuitry shows that it consists of three main elements: a constant current source, an analog switch, and a servo amp.

As shown in the figure, the circuit is configured for idle (or anneal) bias. The servo amp is connected as a simple follower and maintains the gate voltage of the DUT at some desired voltage, the source of the DUT is directly connected to a voltage source, and the constant current source is programmed to an off condition (no current).

During a test, the analog switch is re-programmed so that the servo amp feed-back comes from the DUT source pin. Simultaneously, the VSidle voltage source will be removed from the source pin. Then, as the constant current source is programmed to different values, the gate voltage will be automatically adjusted to maintain the desired source voltage. An A/D reading of the gate voltage will then read the gate voltage for that current.

The compliance limit shown on the figure is a second feed-back path for the servo amp. If the amp tries to adjust the gate voltage beyond certain programmed limits, the compliance limit path will be turned on and limit the swing. Note that this prevents the servo amp from saturating so that it can recover quickly once the condition causing the limit is removed.

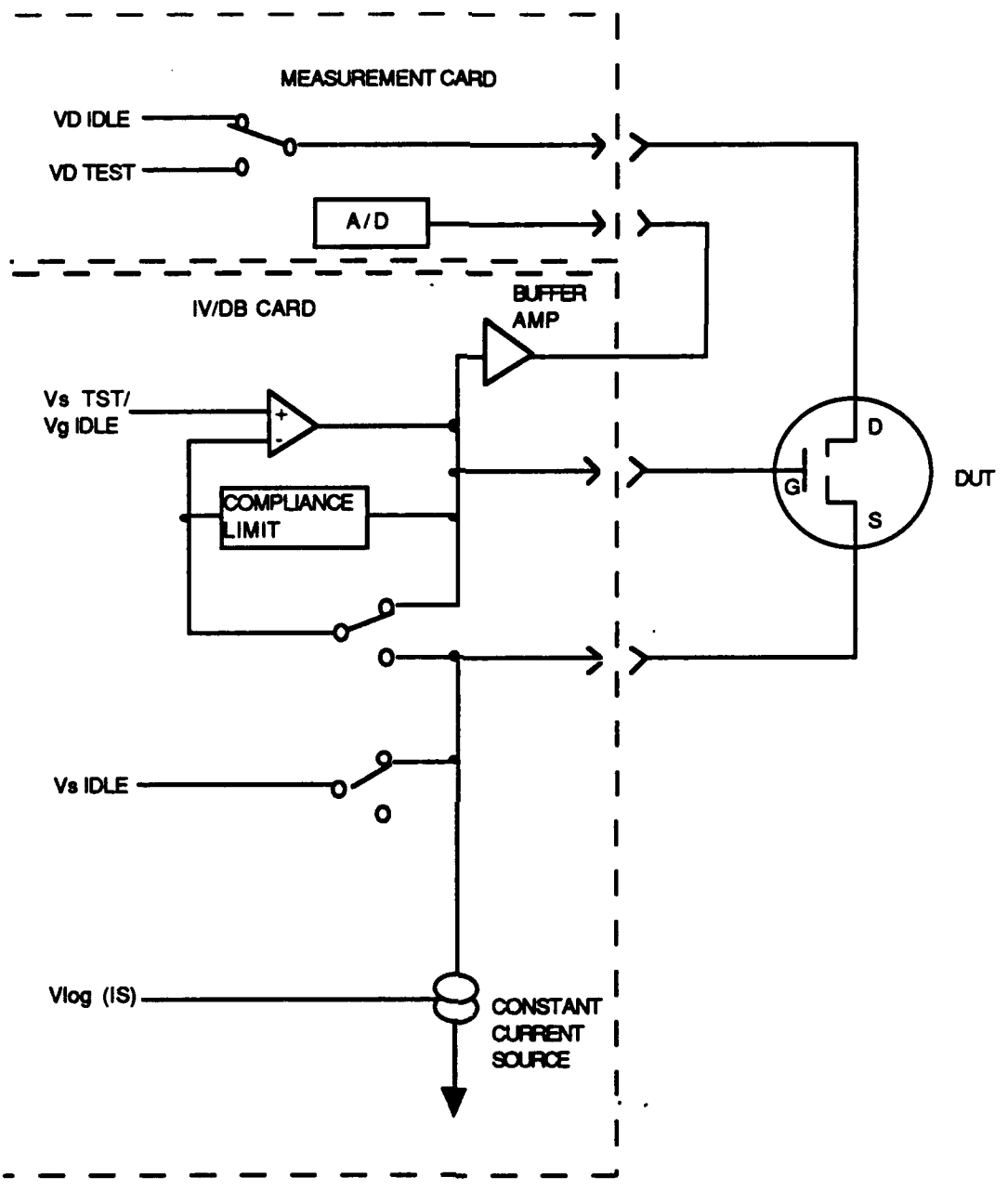

FIGURE 5. FORCE CURRENT, MEASURE VOLTAGE BLOCK DIAGRAM

The two force current/servo voltage circuits are shown in detail on the drawing. Since they are functionally identical, only the one for odd channels will be described.

The constant current source consists of two complementary FET transistors (one N channel - Q12 and one P channel - Q11) and three diodes (D12, D13, D14). The FETs are connected so that their drains are tied together and go to the source connector of the DUT.

Their gates are also tied together and go to the Vs(test) voltage input. Thus, when the gate servo circuit is in a stable condition, there should be 0 volts between the common gate and common drain nodes. The current is set in the circuit by programming a voltage between the gate pins and the end of the diode strings which are connected to the sources of the FETs. The relationship between the applied voltage and resultant current is logarithmic due to the I/V characteristics of the diodes and turn on characteristics of the FETs. The diodes were added to the circuit both to prevent reverse leakage through parasitic diodes in the FETs and to increase and equalize the amount of voltage which must be applied in each direction for maximum current. The FETs and diodes are located inside a PC mounted oven to stabilize the I/V characteristics of the circuit.

U8 and associated circuitry comprises an adder/subtractor which maintains a constant differential voltage across the constant current source for various source test voltages. During testing, the output of the circuit will be Vs(Test) + Vlog(Is). Potentiometer VR4 is adjusted so that this relationship is maintained for all values of Vs(Test). During idle bias, the Vlog(Is) input to the circuit is broken and the circuit becomes a simple follower.

The servo amp consists of U9, transistors Q13 - Q16, and associated circuitry. Transistors Q13 and Q15 serve to provide +/- 15 volt supply voltages to U9. Current flowing into the power supply pins of U9 generate voltage across R56, D18 and R46, D15 which in turn provide bias for the output transistors Q14 and Q16. DC feedback between the U9 and the discrete gain stage is provided by R49 and R50. Essentially, as the output voltage of U9 increases (or decreases), current flowing in the respective supply pin increases. This causes an increase in the voltage drop across R56, D18 (R46, D15) which turns on the output transistor Q16 (Q14) harder, increasing (decreasing) the output voltage and reducing the amount of output current from the output pin of U9.

The voltage gain of the discrete stage is essentially the ratio of R49 and R50 which is 10. This additional loop gain is rolled off at high frequencies to prevent oscillations. A pole-zero compensating circuit is formed by the combination of R49, R50 along with C47, C48.

Feedback for the servo amp is provided through analog switch U10. In the idle mode, gate output voltage is feed back directly, and

in the measurement mode feedback comes from the source pin of the DUT. The idle voltage feedback is divided by the resistive divider R53, R67, VR5, and R63 which divides the feedback voltage by approximately 1/2. This was done because the DAC output which programs the Vg(Idle) voltage has a range of +/-10V whereas the desired idle gate voltage has a range of +/-20V.

U13 and associated circuitry provides the buffered signal for the A/D convertor which is located on the measurement card. The resistive divider converts the +/-20V gate signal to a +/-5V signal which is the range of the A/D convertor used. Potentiometer VR5 provides for fine gain control of the A/D, and potentiometer VR6 provides for offset adjustment.

The desired voltage compliance limit for the gate servo amp comes from the measurement card as a voltage between 0 and 10V. It is amplified by +2 by U11 and by -2 by U12 to generate complimentary voltages between 0 -> +20V and 0 -> -20V. These voltages are applied directly to the bases and through resistors to the collectors of Q17 and Q18. These transistors are normally turned off and the diodes D16 and D17 which are connected between them and the VG Servo line are reverse biased. When the VG Servo signal exceeds the programmed voltage, one of the diodes will become forward biased, turning on its respective transistor and providing a low impedance feedback path for the op amp circuit.

OPERATING INSTRUCTIONS

Fast channels can be programmed and used similar to other channels. There are some small differences which are described below.

EDIT - The EDIT program can be utilized with FAST cards exactly the same as with other cards. The choices for starting times, currents to be forced, and the settling time associated with each current range are slightly different. The EDIT program has built-in checks for valid entries.

CAL - There are several differences in calibrating fast cards. These are noted below:

V-REF ADJUSTMENT - VR1, located on the measurement card, should be adjusted to yield 10.23 volts at TP1. This should be done before running the calibration program.

DAC ADJUSTMENT - There are 7 DAC outputs which are calibrated in this step as opposed to the 4 on other cards.

A/D CALIBRATION - The pots for adjusting the gain and offset of the A/D convertor are located on the IVDB board as opposed to the measurement card on other cards. For even channels, VR2 adjusts the gain and VR3 adjusts the offset. For odd channels, VR5 adjusts the gain and VR6 adjusts the offset. Adjust these pots while observing the screen as with other cards.

CURRENT OFFSET CALIBRATION - For this type of card, the cal program will display a screen which shows three measured numbers and the difference between them. The appropriate lofs pot should be adjusted (VR1 for even channels, VR4

for odd channels) until the readings are all nearly the same.

I/V CALIBRATION - The constant current circuit is logarithmic in nature (linearly varying input voltage causes a logarithmically varying current), but the system calibrates it for every decade of current. Basically, a resistor of known value is placed between the gate and source leads and the Vlog(Is) is varied to produce gate voltages between 1 and 10 volts. Once enough I/V pairs have been collected, the computer performs a least-squares fit to the logarithmic data to generate an equation of the form:

$$V = K1 + k2 * Vlog(Is) + K3 * Vlog(Is)^2$$

This is done for both polarities of current and all the sets of Ks are stored. During test generation, the Ks are used to generate the required voltage to cause the constant current source to output the desired currents.

If a calibration box is used, it will automatically step through the resistors, draw the measured points on the screen, and overlay them with the fitted curve. If manual calibration is done, it will be necessary to insert the resistors manually.

TEST - There is no difference in the way fast cards are used during a test. However, it should be remembered that data is measured much faster with this card than with older cards. It is strongly suggested that fixture capacitance be minimized to insure valid data is taken. If possible, plug the personality card directly into the back of the control unit and avoid the use of extender cables.

It is also suggested that test files be generated and exercised well before an actual test. We have found it helpful to use a digitizing oscilloscope on the gate lead during initial test generation to verify sweep timing details. (NOTE: do not put a scope probe on the source lead as this will significantly lengthen the required settling time for low currents.)

CONCLUSIONS

A fast measurement channel was developed for the TATS system. The new channels are approximately 50 times faster than the original channels. They can be intermixed with all existing TATS cards to allow simultaneous testing of a wide variety of parameters.